**ANALYSIS OF CASCADED H-BRIDGE MULTILEVEL INVERTER CONFIGURATION WITH DOUBLE LEVEL CIRCUIT**

**ABSTRACT**

In this study, a new multilevel inverter configuration which introduces a combination of cascaded H-bridge multilevel inverter with a double level circuit is proposed. The double level circuit is a half-bridge inverter when combined with a cascaded H-bridge multilevel inverter, will increase the output voltage level to nearly twice that of a conventional cascaded H-bridge multilevel inverter. The effectiveness of the proposed configuration is demonstrated with five different cases of cascaded Hbridge multilevel inverter configurations. Phase disposition carriers arrangement with sinusoidal reference has been utilised in pulse width modulation for generating the gating signal of switches to achieve high-quality output voltage waveform. A comparison is carried out with different parameters such as %total harmonic distortion, distortion factor, the maximum voltage step of output voltage level and peak inverse voltage. Analysis of power loss and theoretical calculation of %total harmonic distortion is described. Also, a new method for calculating the overall component count is discussed. As a result, the proposed configuration requires lesser component count for generating higher output voltage level with lower %total harmonic distortion. Selected simulation and experimental results are shown to verify and validate the proposed multilevel inverter configuration.

**BLOCK DIAGRAM FOR PROPOSED SYSTEM**

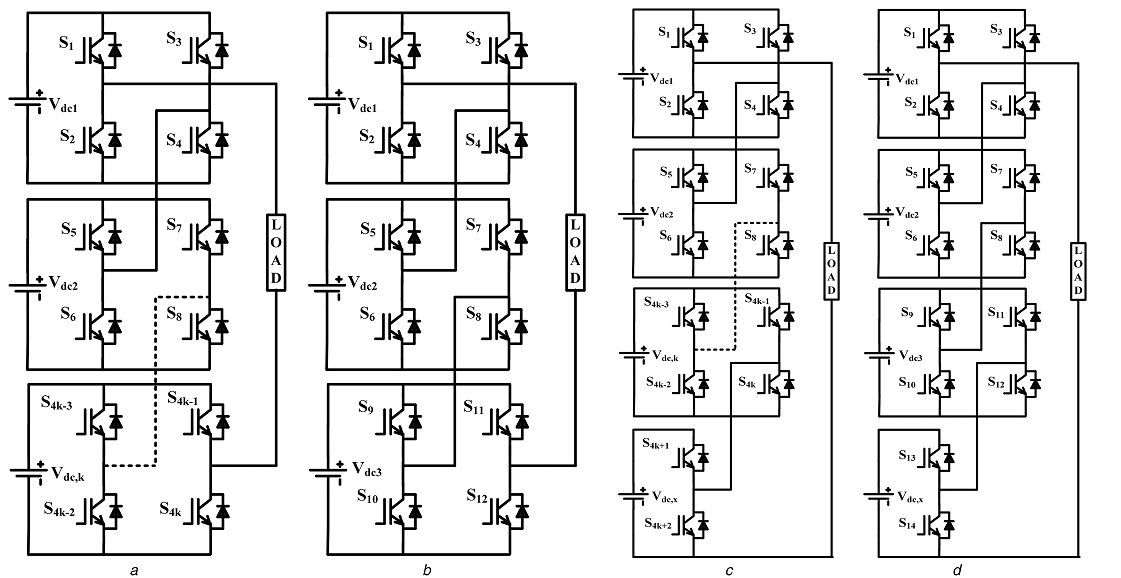


Fig. 1 Proposed topology of MLI (a) Generalised CHBMLI, (b) CHBMLI configuration with three DC sources, (c) Generalised proposed MLI configurations, (d) Proposed MLI configuration with three CHBMLIs.

**DESIGNG SOFTWARE AND TOOLS:**

MAT LAB /SIMULATION Software and simu power systems tools are used. Mainly control system tools, power electronics and electrical elements tools are used.